#mSoC
THE RACE TO 1 PER MILLION
Over all architecture fundamentals

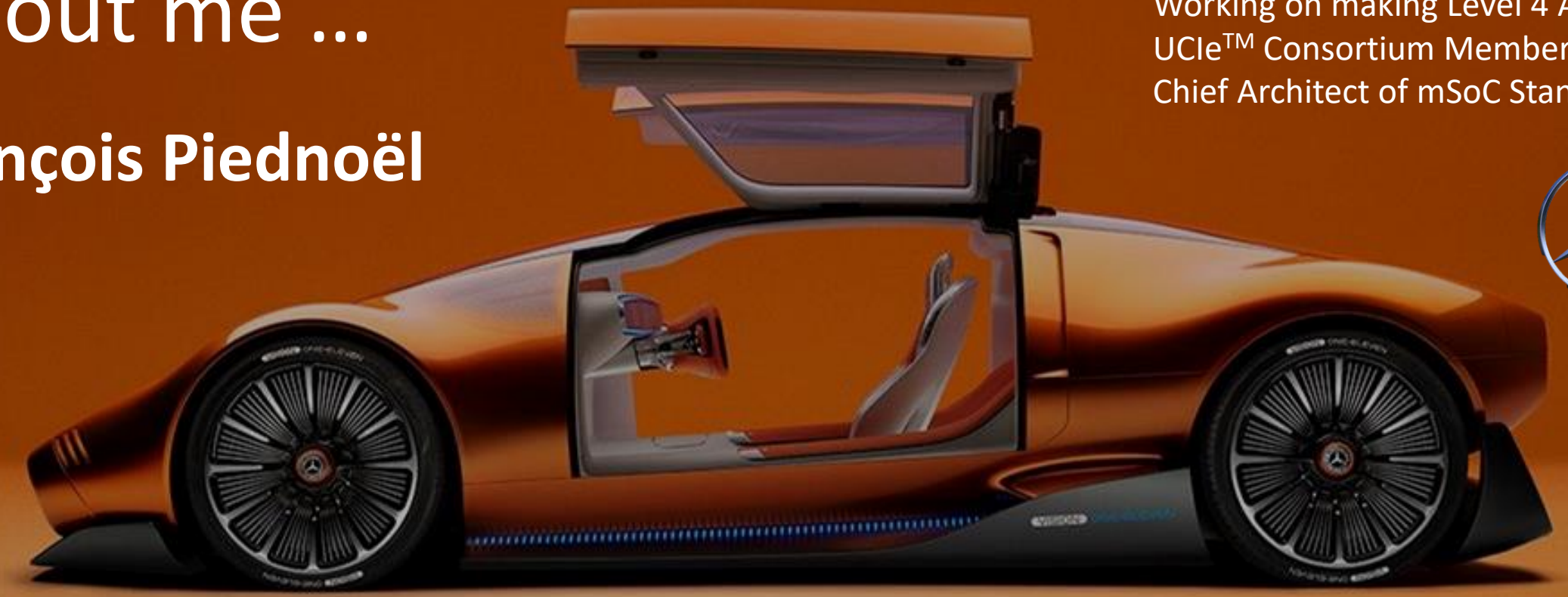
ISO 26262

Engineering Presentation for UCIe

About me …

François Piednoël

4.6 Years at Mercedes-Benz:
Working on making Level 4 Autonomy
UCIe™ Consortium Member
Chief Architect of mSoC Standard



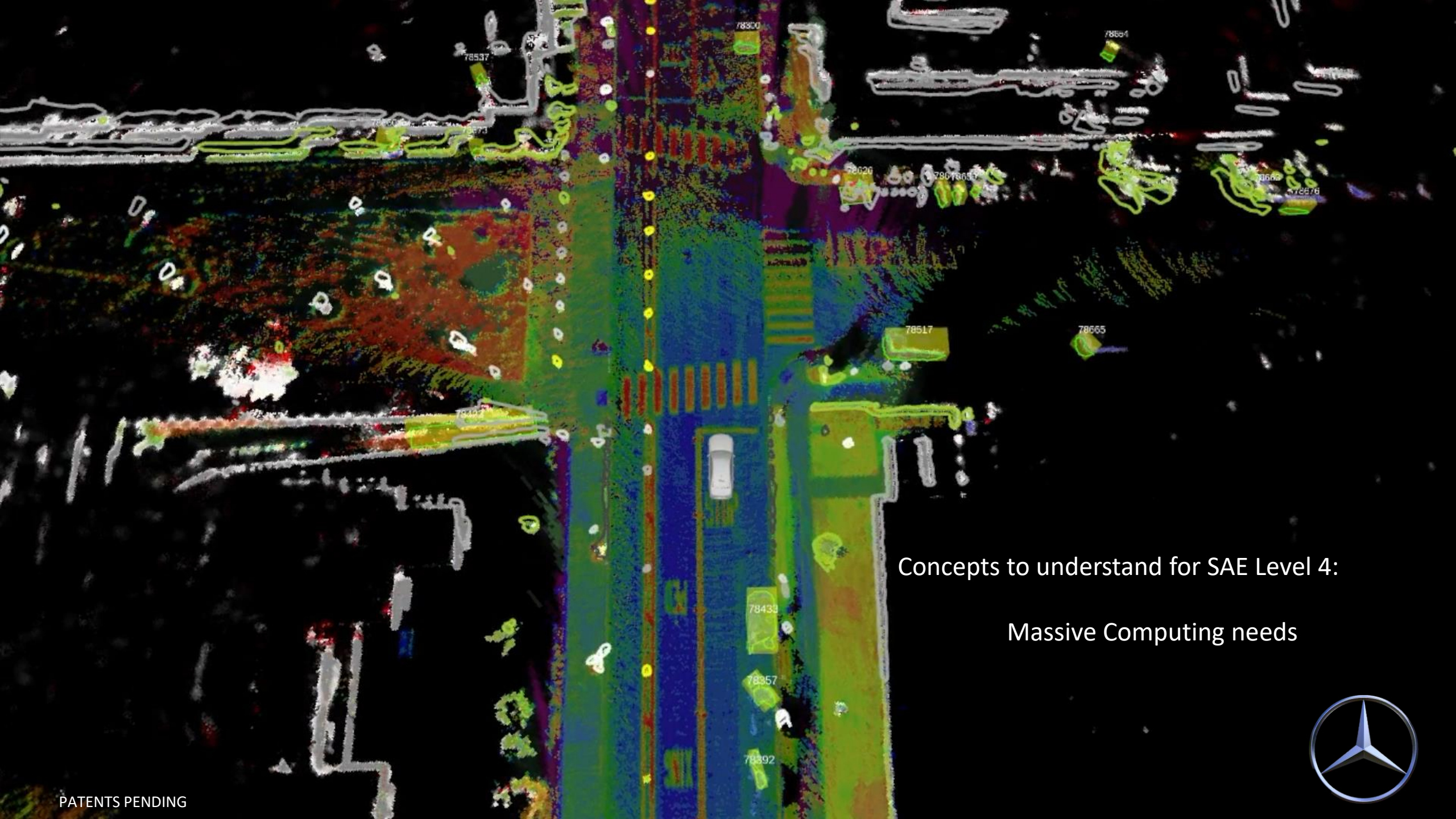
20 years at Intel, Bluetooth in 1997…
Creation of the Pentium IV extreme Edition Product line
Performance Lead Architect for 11 years, Conroe to Skylake
Lead of SKULLTRAIL Platform

Developing the mSoC standard

- A market of automotive grade Chiplet:
- UCIe compliant interconnect.
- ASIL D (except physical fire)
- Optimized for Automotive ML workloads.
- Deterministic Fusion.

PATENTS PENDING

* mSoC: multiple System on C

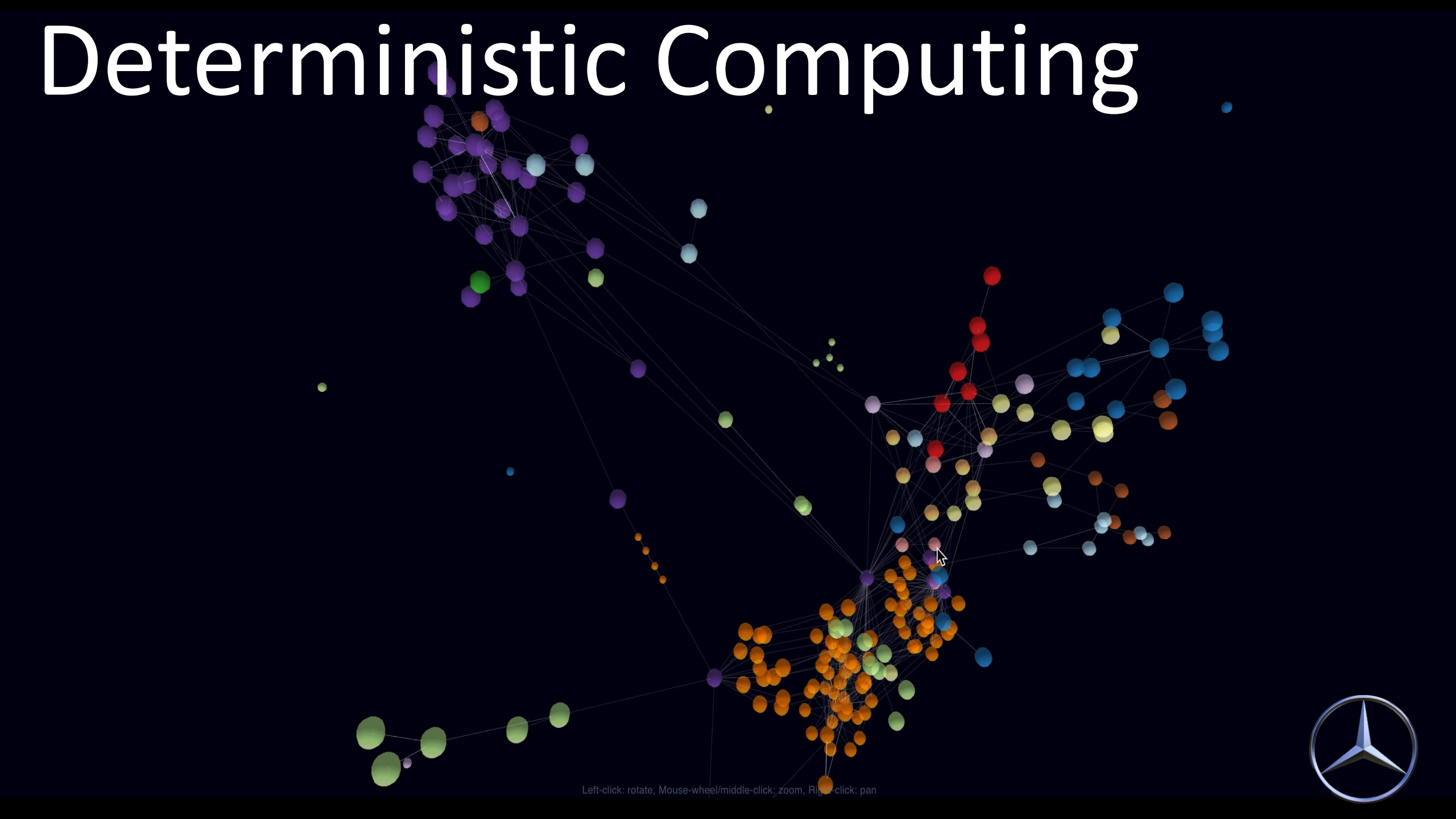


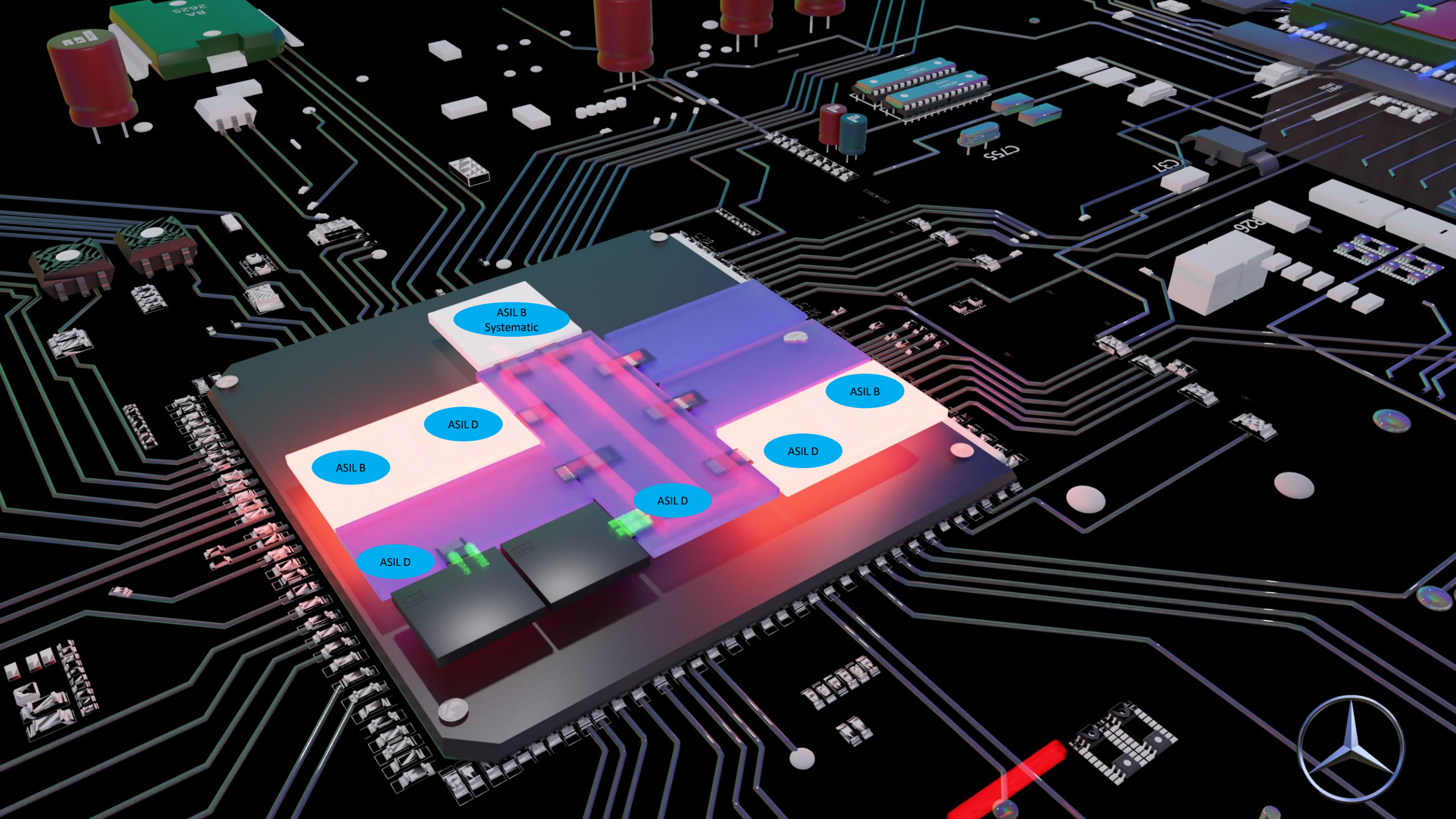
Concepts to understand for SAE Level 4:

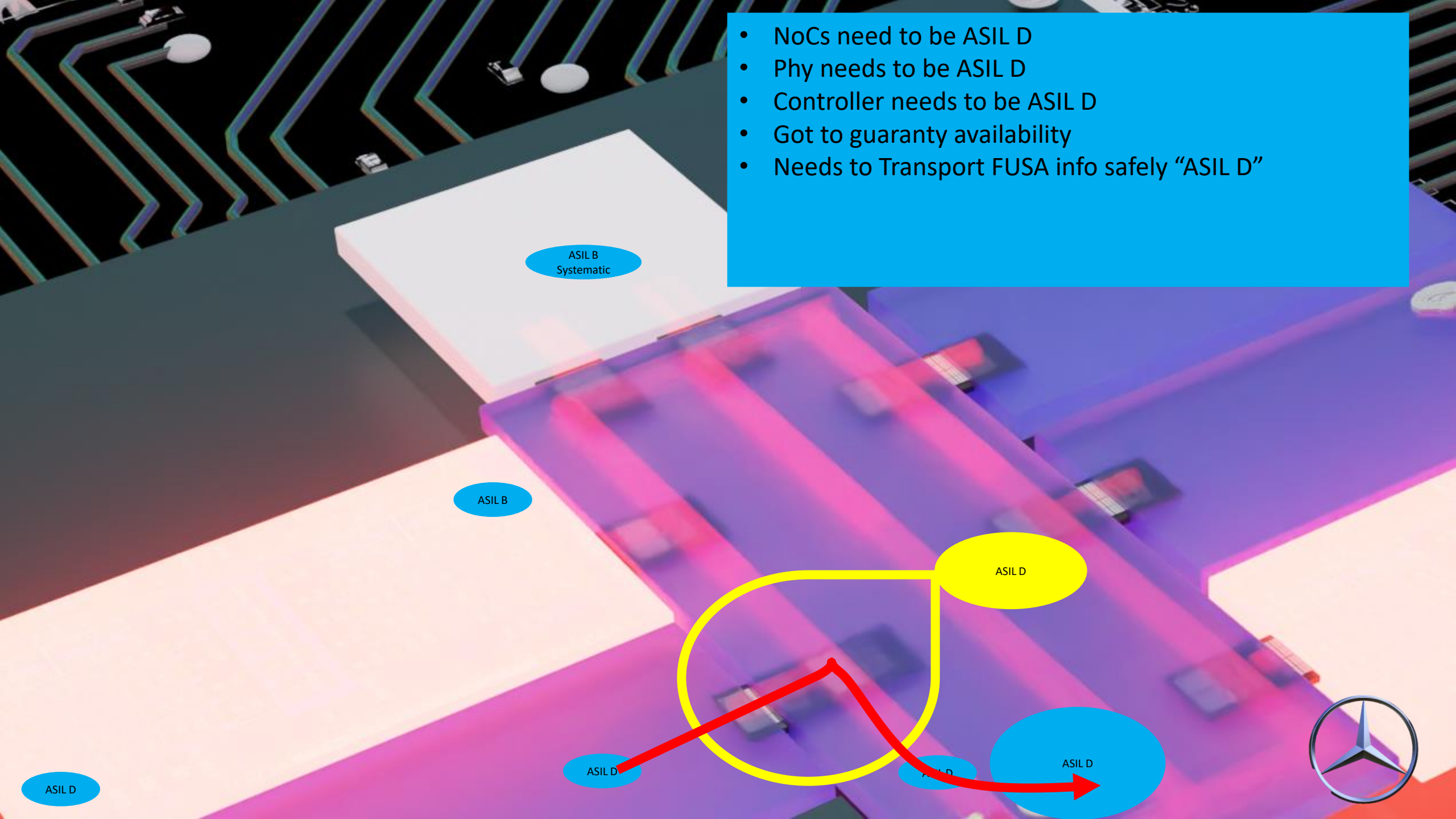
Massive Computing needs

PATENTS PENDING

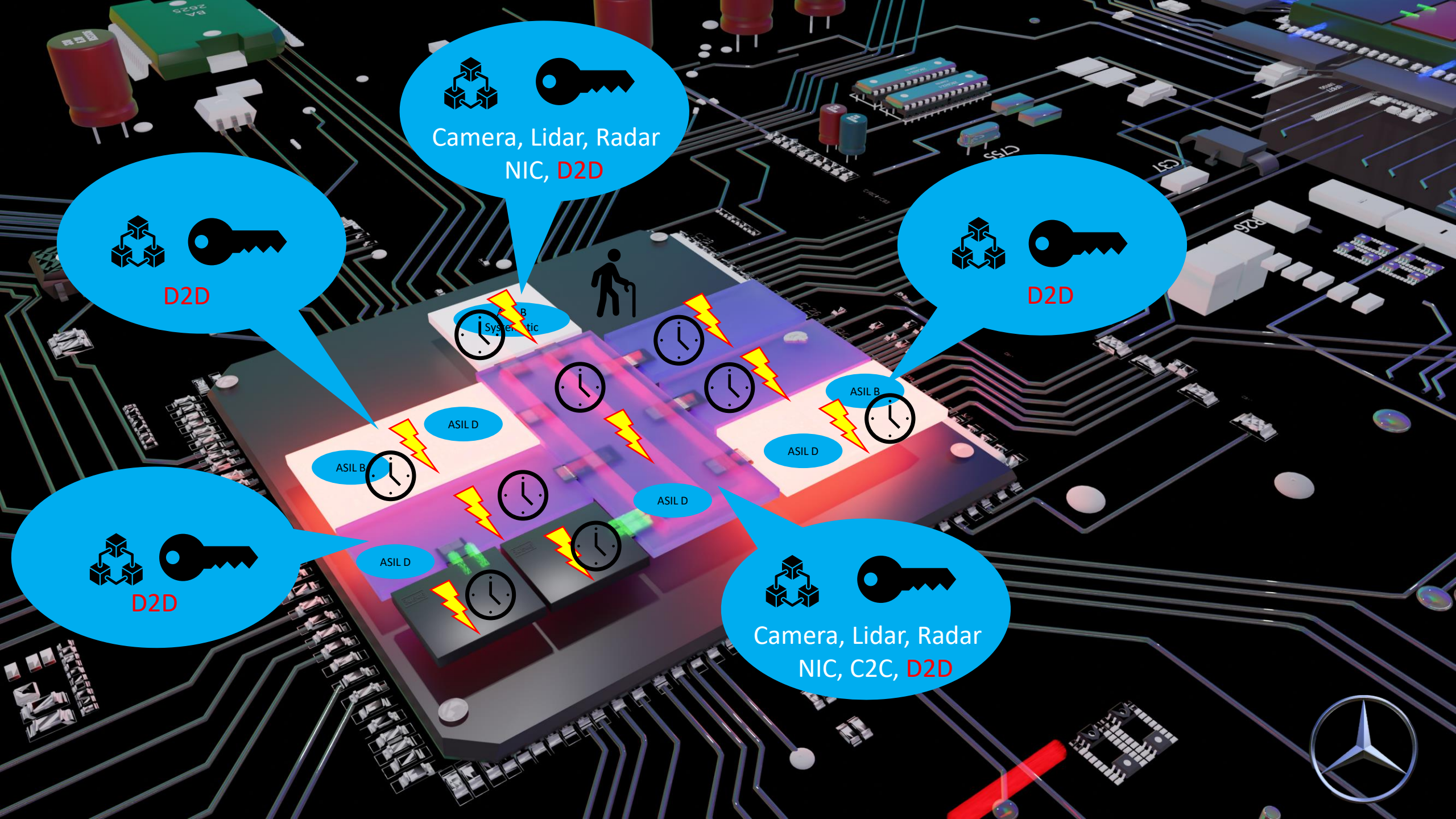
Deterministic Computing



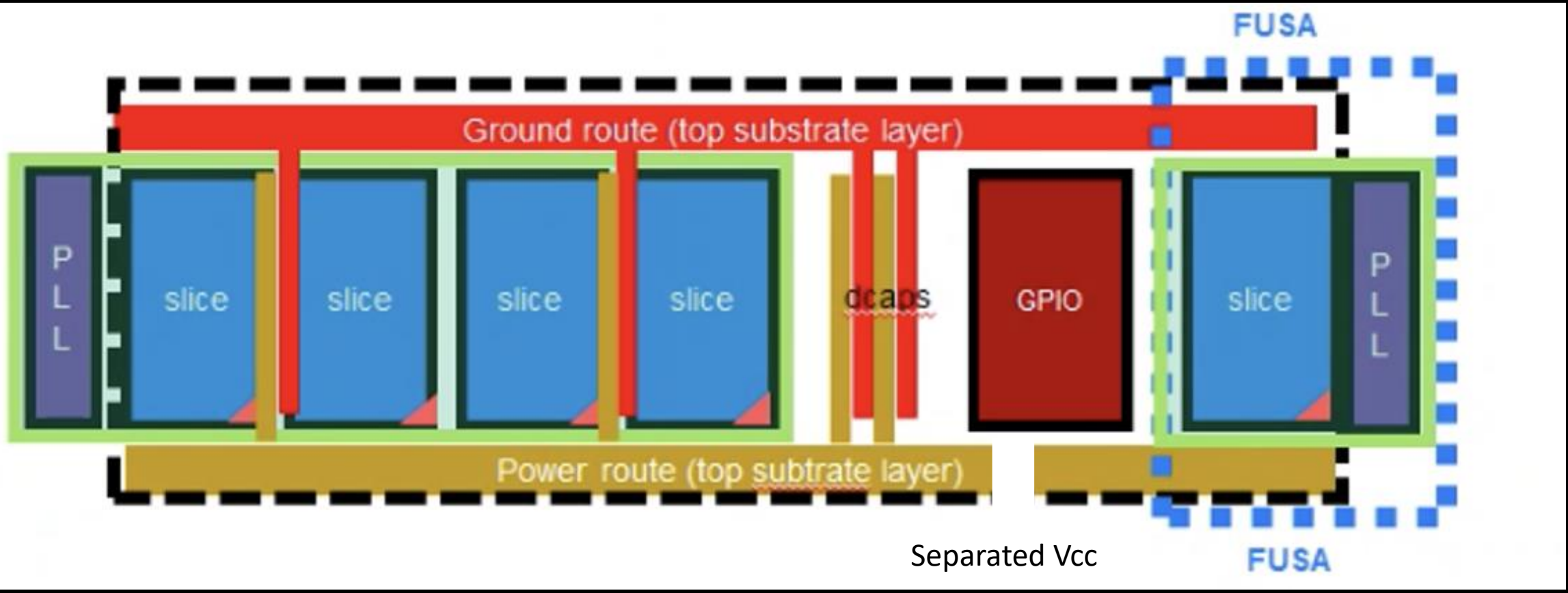

ASIL B
Systematic
ASIL D
ASIL B
ASIL B
ASIL D
ASIL D
ASIL D



- NoCs need to be ASIL D
- Phy needs to be ASIL D
- Controller needs to be ASIL D
- Got to guaranty availability
- Needs to Transport FUSA info safely “ASIL D”


Camera, Lidar, Radar
NIC, D2D
D2D
D2D
D2D
Camera, Lidar, Radar
NIC, C2C, D2D
ASIL B
ASIL D
ASIL B
ASIL D
ASIL D

ASIL D FUSA with Perf Net.



Questions ?

francois.piednoel@Mercedes-benz.com